REMARKS

Claims 1 through 62 are currently pending in the application. Claims 47 through 62 have been withdrawn from consideration. Claims 1 through 46 are subject to an Election of Species Restriction Requirement.

Eight species of invention have been identified by the Examiner including Species III-VIII which have been identified by the Examiner as subspecies of Species I. Applicant notes that species VI has been identified as "[f]orming *notch-shaped* channels asymmetrically with respect to the geographical outline of the semiconductor device to align such a semiconductor device, as shown in Figure 5B;" species VII has been identified as "[f]orming a first size *notch-shaped* channel and a second size notch-shaped channel to align such a semiconductor device, as shown in Figure 5C;" and that species VIII has been identified as "forming a first *notch-shaped* channel in a diagonal direction with respect to a second size *notch-shaped* channel to align such a semiconductor device, as shown in Figure 3." (Office Action, pages 2-3, emphasis added).

Applicant respectfully submits that none of FIGS. 3, 5B or 5C show a *notch-shaped* channel as defined in the present application. Applicant, therefore, assumes that the Examiner was referring generally to the channels shown in FIGS. 3, 5B and 5C with regard to their specific arrangements and configurations as shown in each respective Figure.

As such, Applicant hereby elects, without traverse, to prosecute the invention of species III, which is identified by the Examiner as a subspecies of species I, as set forth in claims 1, 3-8, 10-16, 24, 26-31 and 33-39 and as illustrated in drawing FIGS. 6A (species I) and 4A (species III).

Applicant considers claims 1, 3, 4, 20, 21, 24, 26, 27 and 35 to be generic, and notes that upon allowance of a generic claim, claims depending therefrom in a non-elected species (i.e., claims 2, 9, 17-23, 25, 32, and 40-46) would also be allowable.

Applicant requests an action on the merits of claims 1, 3-8, 10-16, 24, 26-31 and 33-39.

Previously Submitted Information Disclosure Statements

Please note that Information Disclosure Statements were filed in the above-referenced application on September 12, 2001 and October 23, 2002, but that initialed copies of the Form PTO-1449s that accompanied that Information Disclosure Statements have not yet been returned to the undersigned attorney. It is respectfully requested that the information cited in the

Information Disclosure Statements and listed on the Form PTO-1449s be considered and made of record in the above-referenced application and that initialed copies of the Form PTO-1449s evidencing such consideration be returned to the undersigned attorney.

First Preliminary Amendment

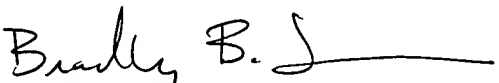
Applicant's undersigned attorney notes the filing herein of a Preliminary Amendment on February 11, 2002, which filing was not acknowledged in the outstanding Office Action. Should the Preliminary Amendment have failed for some reason to have been entered in the Office file, Applicant's undersigned attorney will be happy to have a true copy thereof hand-delivered to the Examiner. The amendments to the claims herein presuppose the entry of the Preliminary Amendment mailed on February 11, 2002.

ENTRY OF AMENDMENTS

The amendments to claims 1, 2, 5, 11, 18-25, 28, 34, 36, 41-46 should be entered because they are supported by the as-filed specification and because they do not introduce new matter to the application.

Applicant again requests entry of the amendments as set forth herein prior to examination of the application on the merits. In view of the foregoing, it is respectfully requested that each of claims 1, 3-8, 10-16, 24, 26-31 and 33-39 be considered on the merits.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

1. (Twice Amended) A method for aligning a semiconductor device with a carrier substrate for electrical interconnection therebetween, the method comprising:

forming at least two [apertures] channels through the semiconductor device from a first major surface thereof to a second, opposing major surface thereof;

providing a major surface of the carrier substrate with at least two alignment features spaced and positioned in respective correspondence to the at least two [apertures] channels;

placing the semiconductor device over the carrier substrate; and

aligning the at least two [apertures] channels formed in the semiconductor device with the at least two alignment features of the carrier substrate.

2. (Twice Amended) The method of claim 1, wherein aligning the at least two [apertures] channels with the at least two alignment features includes sighting each alignment feature of the at least two alignment features through a respective corresponding [aperture] channel of the at least two [apertures] channels.

5. (Amended) The method of claim 3, wherein aligning the at least two [apertures] channels with the at least two alignment features includes placing pins through the at least two [apertures] channels and into the at least two holes.

11. (Amended) The method of claim 5, further comprising removing the pins subsequent to the alignment of the at least two [apertures] channels with the at least two alignment features.

13. The method of claim 12, wherein the pick and place device is used to align the semiconductor device with the carrier substrate by inserting pins carried by a head of the pick and place device through the at least two [apertures] channels and the at least two holes.

18. (Amended) The method of claim 17, further comprising aligning the at least two [apertures] channels with the at least two alignment features by sighting the optically perceptible marks on the carrier substrate through the at least two [apertures] channels of the semiconductor device.

19. (Amended) The method of claim 18, wherein sighting the optically perceptible marks on the carrier substrate through the at least two [apertures] channels includes sighting the optically perceptible marks with an optical instrument.

20. (Amended) The method of claim 1, wherein the at least two [apertures] channels are each defined by a diameter and wherein the method further comprises forming at least one of the at least two [apertures] channels with a larger diameter than that of at least one other [aperture] channel of the at least two [apertures] channels.

21. (Twice Amended) The method of claim 20, wherein providing the major surface of the carrier substrate with at least two alignment features includes correlating a size of each of the at least two alignment features with a size of a respectively corresponding [aperture] channel of the at least two [apertures] channels.

22. (Amended) The method of claim 1, wherein forming the at least two [apertures] channels includes forming the at least two [apertures] channels in an asymmetrical pattern on the semiconductor device.

23. (Amended) The method of claim 1, wherein forming the at least two [apertures] channels includes forming at least one notch on a periphery of the semiconductor device.

24. (Twice Amended) A method of testing a semiconductor device having a plurality of discrete conductive elements disposed in a pattern on a surface thereof, the method comprising:

providing a carrier substrate having a plurality of terminal pads arranged in a pattern corresponding to a mirror image of the pattern of discrete conductive elements;

forming at least two [apertures] channels in the semiconductor device, each [aperture] channel passing from a first surface thereof to a second, opposing surface thereof;

providing the carrier substrate with at least two alignment features, each alignment feature respectively spaced and positioned in correspondence to one of the at least two [apertures] channels;

placing the semiconductor device over the carrier substrate;

aligning each [aperture] channel of the at least two [apertures] channels formed in the semiconductor device with a corresponding alignment feature of the at least two alignment features of the carrier substrate;

electrically contacting each discrete conductive element of the plurality with a terminal pad of the plurality; and

passing at least one electrical signal between the semiconductor device and the carrier substrate.

25. (Twice Amended) The method of claim 24, wherein aligning each of the at least two [apertures] channels with a corresponding alignment feature of the at least two alignment features includes sighting each alignment feature through a corresponding [aperture] channel.

28. (Twice Amended) The method of claim 26, wherein aligning each of the at least two [apertures] channels with a corresponding alignment feature of the at least two alignment features includes placing pins through the at least two [apertures] channels and into the at least two holes.

34. (Twice Amended) The method of claim 29, further comprising removing the pins subsequent to the alignment of each of the at least two [apertures] channels with a corresponding alignment feature of the at least two alignment features.

36. (Amended) The method of claim 35, wherein the pick and place device is used by placing pins carried by a head of the pick and place device through the at least two [apertures] channels and the at least two holes.

41. (Amended) The method of claim 40, further comprising aligning the at least two [apertures] channels with the at least two alignment features by sighting the at least two optically perceptible marks on the carrier substrate through the at least two [apertures] channels of the semiconductor device.

42. (Twice Amended) The method of claim 41, wherein sighting the at least two optically perceptible marks on the carrier substrate through the at least two [apertures] channels is effected using an optical instrument.

43. (Twice Amended) The method of claim 25, wherein the at least two [apertures] channels are each defined by a diameter and wherein the method further comprises forming at least one of the at least two [apertures] channels with a larger diameter than that of at least one other [aperture] channel of the at least two [apertures] channels.

44. (Twice Amended) The method of claim 43, wherein providing at least two alignment features on the carrier substrate includes correlating a size of each alignment feature of the at least two alignment features with a size of a corresponding [aperture] channel of the at least two [apertures] channels.

45. (Amended) The method of claim 25, wherein forming the at least two [apertures] channels includes forming the at least two [apertures] channels in an asymmetrical pattern on the semiconductor device.

46. (Amended) The method of claim 25, wherein forming the at least two [apertures] channels includes forming at least one notch on a periphery of the semiconductor device.